Digital LLRF Technology on a µTCA Platform

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Introduction

The storage ring of the Advanced Photon Source (APS) at Argonne National Laboratory uses radiofrequency (RF) systems to maintain the energy levels of its circulating electron beam. These RF systems use feedback control systems to manage the amplitude and phase of the accelerating voltage in the RF cavities. Currently, the low-level RF systems (LLRF) use analog hardware, but the long-term goal is to migrate to digital LLRF technology.

Therefore, the APS is testing the possibility of using a digital, µTCA platform. Previous RF filters have been developed using National Instruments hardware and development tools. Using a µTCA platform offers access to a larger ecosystem of manufacturers and vendors that adhere to this specification. Using FPGA Mezzanine Card (FMC) Carrier Boards also enables the user to easily switch out the modules in the FMC slots as needed.

Hardware Components

- FPGA Mezzanine Card Carrier
  - Xilinx Kintex-7 FPGA
- FMC 1: Four 16-bit, 2 MSPS analog-to-digital (ADC) converters
- FMC 2: Four 18-bit, 1 MSPS digital-to-analog (DAC) converters

VHDL Design

The main task for the VHDL code in the FPGA is to provide a functional serial peripheral interface with the ADC's and the DAC's. The hardware is designed to meet the timing specifications and provide the control signals necessary to operate the signal conversions.

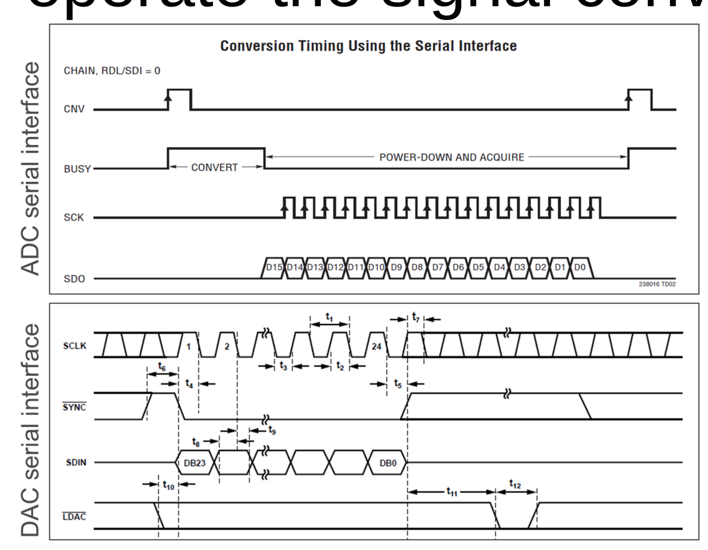


Figure 1: Serial interface diagrams for the ADC and the DAC. VHDL code was designed to implement these waveforms and timing.

ADC Data Analysis

Two tools were employed to analyze data collected from the ADC. Fast Fourier transform (FFT) is an algorithm that decomposes a sampled, discrete-time signal into its component frequencies and their relative amplitudes [dBV]. The power spectral density [dBV^2/Hz] measures a signal's power intensity in the frequency domain.

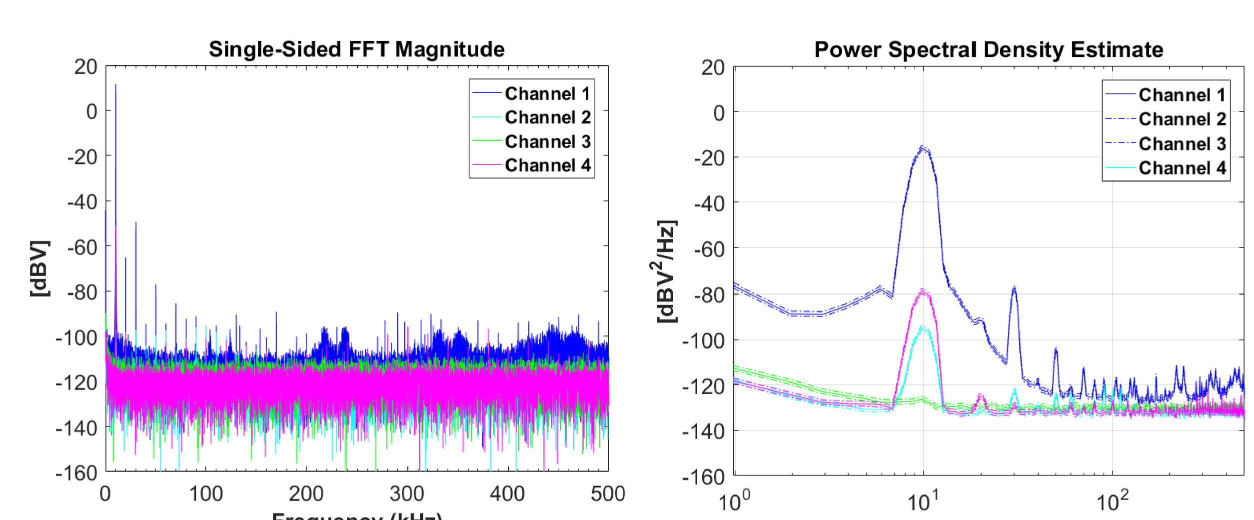


Figure 2: (a) 32K point FFT. (b) Power spectral Density graph. Input was a 10 kHz full-scale sinusoidal signal on channel 1.

DAC Data Analysis

For testing, signals were fed into the ADC, through the FPGA, and directly output through the DAC.

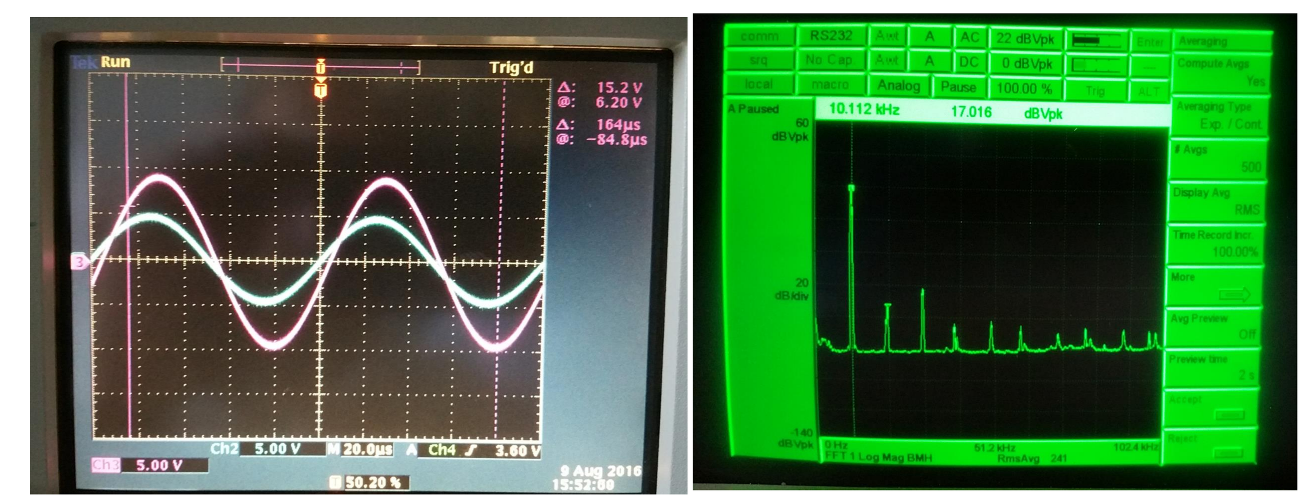


Figure 3: (a) The input signal to the ADC is shown in cyan, while the output signal from the DAC is shown in magenta. (b) An FFT of the signal input.

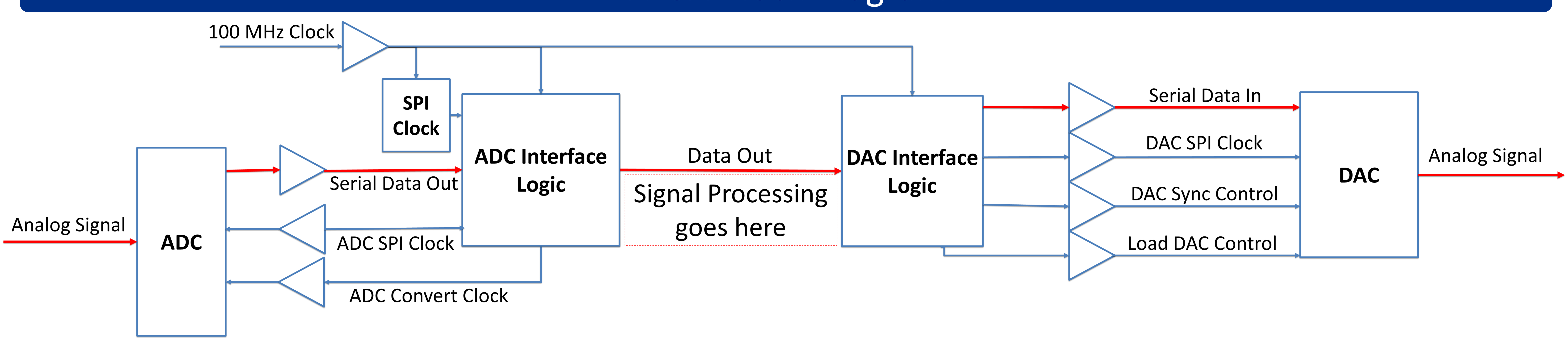
Conclusions/Future Work

We successfully demonstrated use of ADC and DAC modules on a µTCA FMC carrier for baseband signal acquisition. The next step would be to implement signal processing with the FPGA. Ultimately, full digital LLRF will require transition from baseband to intermediate frequency signals.

References

[1] E. Cunningham, *Digital Filtering: An Introduction*. Boston, MA: Houghton Mifflin Company, 1992.

FPGA Block Diagram



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